WHAT IS CLAIMED IS:

1. A method of operating a switch matrix comprising:

configuring said switch matrix to couple a first input to a first output;

receiving an information stream at said first input, wherein said information stream contains a plurality of portions in a sequence and a one of said plurality of portions is in one position in said sequence; and

reconfiguring said switch matrix during a first time period, said first time period corresponding to said one position in said sequence.

2. The method of claim 1, wherein said reconfiguring couples said first input to a second output.

3. The method of claim 2, wherein said switch matrix is a rearrangeably non-blocking switch matrix.

4. The method of claim 2, wherein said switching matrix is a CLOS switching matrix.

5. The method of claim 4, wherein said method avoids generating an error in other information streams transiting said switch matrix during said reconfiguring.

6. The method of claim 2, further comprising:

re-arranging certain ones of said plurality of portions such that said one of said plurality of portions is in another position in said sequence, wherein said first time period corresponds instead to said another position.

7. The method of claim 6, wherein said information stream is a SONET frame.

8. The method of claim 6, wherein said first portion contains network protocol overhead.

9. The method of claim 6, wherein said information stream is carried by a signal, further comprising:

loading said one of said plurality of portions with a value, said value enabling said matrix to synchronize with said signal more easily.

10. The method of claim 2, wherein a number of said plurality of portions are in various positions in said sequence, said number of said plurality of portions including said one of said plurality of portions, said method further comprising:

re-arranging certain ones of said plurality of portions prior to said receiving such that said number of said plurality of portions are in a set of contiguous positions, wherein said first time period corresponds instead to said set of contiguous positions.

11. The method of claim 10, further comprising:

re-arranging said certain ones of said plurality of portions such that said number of said plurality of portions are in their original positions.

12. The method of claim 11, further comprising:

reading protocol information from said one of said plurality of portions during said re-arranging certain ones of said plurality of portions prior to said receiving;

processing said protocol information to derive new protocol information;

writing said new protocol information to said one of said plurality of portions during said re-arranging said certain ones of said plurality of portions.

13. A method of operating a switch matrix comprising:

configuring said switch matrix to couple a plurality of inputs to a plurality of outputs;

receiving a plurality of information streams at said plurality of inputs, wherein

each one of said plurality of information streams comprises a plurality of portions in a sequence and is received at a corresponding one of said plurality of inputs,

for each one of said plurality of information streams,

a one of said plurality of portions is in a specific position of said sequence, and

a time period during which said one of said plurality of portions transits said switching matrix is at least minimally concurrent with said time period for each other one of said plurality of information streams, and

a time period of said minimal concurrency defining a switching period; and

reconfiguring said switch matrix during said switching period.

14. The method of claim 13, wherein said time period of said minimal concurrency is such that, for said each one of said plurality of information streams, a leading edge of said one of said plurality of portions has been output from a corresponding one of said plurality of outputs before a trailing edge of said one of said plurality of portions is received at said corresponding one of said plurality of inputs.

15. The method of claim 13, wherein said configuring couples one of said plurality of inputs to a one of said plurality of outputs and said reconfiguring couples said one of said plurality of inputs to another of said plurality of outputs.

16. The method of claim 13, wherein said switch matrix is a rearrangeably non-blocking switch matrix.

17. The method of claim 13, further comprising:

for certain ones of said plurality of information streams, re-arranging certain ones of said plurality of portions such that said one of said plurality of portions are moved to another position in said sequence of said

plurality of information streams in order to achieve said minimal concurrency.

18. The method of claim 13, wherein, for certain ones of said plurality of information streams, a number of said plurality of portions are in various positions in said sequence, said number of said plurality of portions including said one of said plurality of portions, said method further comprising,:

for said certain ones of said plurality of information streams, re-arranging certain ones of said plurality of portions prior to said receiving such that said number of said plurality of portions are in a set of contiguous positions, wherein a group time period during which said number of said plurality of portions transits said switching matrix is at least minimally concurrent with said group time period for each other one of said certain ones of said plurality of information streams.

19. The method of claim 18, further comprising:

for said certain ones of said plurality of information streams, re-arranging said certain ones of said plurality of portions such that said number of said plurality of portions are in their original positions.

20. A switching apparatus comprising:

a switching matrix, having a matrix input, a control input, and a plurality of matrix outputs, wherein said switching matrix is configured to receive an information stream at said matrix input, said information stream comprising a plurality of portions; and

control circuitry, having a control output coupled to said control input, wherein

said control circuitry is configured to initially configure said switching matrix to output said information stream at a one of said plurality of matrix outputs,

said control circuitry is configured to subsequently configure said switching matrix to output said information stream at another of

said plurality of matrix outputs during a period of time during which said one of said plurality of portions is transiting said switching matrix.

21. The switching apparatus of claim 20, further comprising:

an input resequencing circuit, having a resequencer input and a resequencer output coupled to said matrix input, wherein said input resequencing circuit is configured to

receive said information stream at said resequencer input,

rearrange certain ones of said plurality of portions such that a one of said plurality of portions is moved from an original position in an original sequence of said plurality of portions to another position in said original sequence in order to produce a modified sequence of said plurality of portions, and

provide said information stream to said switching matrix at said input resequencer output.

22. The switching apparatus of claim 21, further comprising:

a first output resequencing circuit, coupled to said one of said plurality of matrix outputs, wherein said first output resequencing circuit is configured to move said one of said plurality of portions from an original position in said modified sequence to a position in said modified sequence corresponding to said original position in said original sequence; and

a second output resequencing circuit, coupled to said another of said plurality of matrix outputs, wherein said second output resequencing circuit is configured to move said one of said plurality of portions from an original position in said modified sequence to a position in said modified sequence corresponding to said original position in said original sequence.

23. The switching apparatus of claim 20, further comprising:
an input resequencing circuit, having a resequencer input and a resequencer output coupled to said matrix input, wherein
said first resequencing circuit is configured to
receive said information stream at said resequencer input,
rearrange certain ones of said plurality of portions such that a number of said plurality of portions occupy a set of contiguous positions in a sequence of said plurality of said portions, and
provide said information to said switching matrix at said first resequencing output,
said number of said plurality of portions including said one of said plurality of portions, and
said subsequent configuration of said switching matrix occurs instead during a period of time during which said number of said plurality of portions is transiting said switching matrix.

24. The switching apparatus of claim 20, wherein said switching matrix is a re-arrangeably non-blocking switching matrix.

25. The switching apparatus of claim 20, wherein said one of said portions is expendable.

26. The switching apparatus of claim 20, wherein said one of said plurality of portions contains protocol overhead information.

27. The switching apparatus of claim 20, wherein
said matrix input is one of a plurality of matrix inputs,
said information stream is one of a plurality of information streams,
each one of said plurality of information streams is received at a corresponding one of said plurality of matrix inputs,

said control circuitry is further configured to further initially configure said switching matrix to couple each one of said plurality of matrix inputs to a corresponding one of said plurality of matrix outputs, and

no errors occur in said plurality of information streams as a result of said subsequent configuration of said switching matrix.

28. The switching apparatus of claim 20, wherein said subsequent configuration of said control circuitry occurs in response to commands from control software running on said control circuitry.

29. The switching apparatus of claim 20, wherein said subsequent configuration of said control circuitry occurs in response to commands from control software running on a route processor coupled to said control circuitry.

30. A switching apparatus comprising:

an input resequencing circuit, having a resequencer input and a resequencer output, wherein said first resequencing circuit is configured to

receive an information stream comprising a plurality of portions at said resequencer input, each one of said plurality of portions comprising a plurality of sub-portions, and

move a one of said plurality of sub-portions of said each one of said plurality of portions from an original position in a sequence of said each one of said plurality of portions to another position in said sequence, and

output said information stream at said resequencer output;

a switching matrix, having a matrix input coupled to receive said information stream from said resequencer output, a control input, and a plurality of matrix outputs; and

control circuitry, having a control output coupled to said control input, wherein said control circuitry is configured to cause said switching matrix to switch said information stream from said one of said plurality

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of matrix outputs to another of said plurality of matrix outputs during a period of time corresponding to said another position.

31. The switching apparatus of claim 30, further comprising:

a first output resequencing circuit, coupled to said one of said plurality of matrix outputs and configured to move said one of said plurality of sub-portions of said each one of said plurality of portions from said another position in said sequence to said original position in said sequence; and

a second output resequencing circuit, coupled to said another of said plurality of matrix outputs and configured to move said one of said plurality of sub-portions of said each one of said plurality of portions from said another position in said sequence to said original position in said sequence.

32. The switching apparatus of claim 30, wherein said switching matrix is a re-arrangeably non-blocking switching matrix.

33. The switching apparatus of claim 30, wherein said one of said portions is expendable.

34. The switching apparatus of claim 30, wherein said one of said plurality of portions contains protocol overhead information.

35. The switching apparatus of claim 30, wherein

said matrix input is one of a plurality of matrix inputs,

said information stream is one of a plurality of information streams,

each one of said plurality of information streams is received at a corresponding one of said plurality of matrix inputs,

said control circuitry is further configured to further initially configure said switching matrix to couple each one of said plurality of matrix inputs to a corresponding one of said plurality of matrix outputs, and

no errors occur in said plurality of information streams as a result of said subsequent configuration of said switching matrix.

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